Electronics procurements

24 October 2014
Geoff Hall
Procurements from CERN

• There are a wide range of electronics items procured by CERN
  – but we are familiar with only some of them

• Probably two main categories:
  – for experiments: mainly, but not only, LHC where users and CERN staff are building their experiments
    • mostly customised items, specific to the project
    • but also less customised parts, such as power supplies, controls, crates, optical links
  – for accelerators:
    • we are less familiar with their requirements, and may be even larger than experiments
    • some of it does resemble experiment procurements, i.e. customised, often located in radiation zones
    • other parts are probably more standard, such as PS, controls, etc
Experiment requirements

- Use examples from CMS – only time for a few illustrations

- Several types of electronics purchases, including:
  - custom integrated circuits (ASICs) – radiation zone
    - sometimes packaged, or custom assemblies
  - multi-layer hybrids (electromechanical support for ASICs) to attach to sensors
    - radiation zone
  - board-based (VME/μTCA/ATCA/...) off-detector digital electronics
    - heavy use of FPGAs, processing and control functions
  - data transmission via high speed optical links, and electrical assembly

- We are by no means responsible for all of them!
  - but hopefully can provide some insight, or links to contacts
  - several technical experts present today
Silicon tracker detectors

- Very large systems in CMS, ATLAS and also LHCb and ALICE

p-n diode arrays, finely segmented into microstrips (pitch ~100µm) assembled into modules with ASICs
Typical module components

Kapton Bias Circuit
Carbon Fiber/Graphite Frame
Silicon Sensors
Front-End Hybrid
APV and control chips
Pins
Pitch Adapter
Kapton cable

Now incorporated with the hybrid.
New types of module under development

- ~15000 modules transmitting
  - $p_T$-stubs to L1 trigger @ 40 MHz
  - full hit data to HLT @ 0.5-1 MHz

~7100 PS-modules

~8400 2S-modules
CMS Tracker ASIC evolution

- 1999: APV25 0.25µm
  - 7 mm x 8mm (128 chan)
- 2011: CBC 0.13µm
  - 7 mm x 4 mm (128 chan)
- 2013: CBC2 0.13µm
  - 11 mm x 5 mm (254 chan)

programmable settings (now standard)
analogue data
~4 µs latency
wire-bondable
pulse-shaping choice

binary data,
6.4 µs latency
wire-bondable

bump-bondable,
cluster & correlation logic
CBC2 C4 wafers

wafer name: A4PNFAH

delivered on wafers, and tested in-house
first wafer probed manually
More advanced hybrids
Some requirements

- Fine pitch
- Dense layout
- Multi-layers
- Impedance control
- ...

Oct 2014 Geoff Hall
Supplemented by off-detector digital boards...

- typical of many other CMS modules
Today’s hardware

MP7 (Virtex-7 XC7VX690T)
future generations will improve, but don’t yet know precisely how

purpose-built µTCA card for CMS upgraded L1 calorimeter trigger
TM performance & calo algorithms demonstrated in recent integration tests

- **72 input/72 output** optical links
- all links operate at **12.5 Gbps**
  (10 Gbps in CMS)
- total bandwidth > **0.9 Tbps**

tested, currently in production

NB good cooling required!
IN
- 72 x 12.5 Gbps
  = 0.9 Tbps

OUT
- 72 x 12.5 Gbps
  = 0.9 Tbps

flexible processing

NB smaller form factor than 9U FED

Power similar
Not always problem-free

• Sensors: two major contracts with very different production quality

• Hybrids: flexible kapton-metal layer structure
  — subtle problems in through-via manufacture identified at late stage

• ASIC yield: variations after initial very good beginning
  — worked with company to understand and solve

• Cooling plant performance: manufacture weakness
  — failures in plant and components which could have had major repercussions

• QA issues – picked up by monitoring, in time
  — early attention to minor details is crucial to avoiding costly delays
  — all highly specialised items with few, or no, second sources
Hybrid cross-section – after actions

Recent cross-sections from company, confirmed by CMS

- Extra kapton layer, reduces glue
- 100µm vias -> 120µm
- New metal process
principally designed with two CMS users in mind

- the **Trigger Control & Distribution System (TCDS)** –

  *distribution of LHC clock*, fast (e.g. trigger) and slow commands, reception of synchronous detector status,…

- the **Pixel Front End Driver (pixFED)**

  - replacement front end board to acquire data from the upgrade pixel detector, to be installed in 2017;

- **compatibility with uTCA for CMS (AMC13)**

- **low jitter clock distribution & deterministic latency**

- **capability to run 10Gbps SERDES links**
**16 layer PCB**
Nelco N4000 13-EPSI
- low loss tangent for HF
- low dielectric constant
- misaligned with PCB weave

strict constraint on thickness
manufacturing experiences

submitted prototype and pre-production series runs with two different manufacturers
  o one well known to CERN/UK, one with no prior experience of
  o experimented with two PCB materials compatible with the impedances & high speed signal integrity required

large fraction of development period dedicated to tracking down & resolving manufacturing issues
  o two manufacturers extremely useful to identify manufacturing vs. design faults (whether due to designer error or board complexity)
  o have learnt the importance of good, two-way communication with your supplier
for 10Gbps we can’t use simple FR4...

**Nelco N4000** laminate (Park) has very good high frequency characteristics but now known to be susceptible to 
**delamination & registration defects**
- also expensive material, low yield
- requires **careful handling during manufacture & assembly**;

**TU-872 SLK** laminate (TUC) trialled successfully but also tends to suffer similar registration defects –

**key is building communicative relationship with supplier**
Two approaches

1. Maintain tower geometry - develop rad-tolerant solutions for 3000 fb^{-1}
   - EE towers e.g. in Shashlik design (crystal scintillator: LYSO, CeF)
   - Te build HE with more fibers, and rad-tolerant scintillator

1. Alternative geometry/concepts
   - Potentially improved performance and/or lower cost
   - Dual fiber read-out: scintillation & Cerenkov (DROC) – alla DREAM/RD52
   - Particle Flow Calorimeter (PFCAL) – following work of CALICE
Upgrade project status

• R&D underway, especially in UK, for at least 5 years
  – prototyping ASICs, board based electronics, detector modules, trigger and readout systems
    • NB includes much FPGA firmware and online software, as well as simulations of future detectors and their physics performance
• New detectors should be installed and be operational in 2023
  – several years of procurement, construction, assembly, qualification, commissioning tests are needed before installation
    • followed by commissioning in the experiment, then operation
  – approval of construction funding is still at an early stage
    • although under discussion for some years
    • Technical Design Reports, for final approval, expected 2016-2017
• R&D funds in place in many agencies
  – expect this to grow further in the coming years